WHAT IS CLAIMED IS:

1. A method of performing integer multiply operations on large integer operands having a first number of bit positions using multi-media instructions that only support parallel multiply operations for small operands having a second number of bit positions, wherein the first number is at least twice as large as the second number, the method comprising:

manipulating the large integer operands to position segments of the large integer operands into register positions used as source fields by the multi-media instructions;

executing a plurality of multi-media parallel multiply instructions to form a series of partial products; and

adding the partial products together to produce an integer result having at least the first number of bit positions.

2. The method of claim 1 wherein the first number of bit positions is 32 or 64, and the second number of bit positions is 16.

3. The method of claim 1 wherein at least one of the plurality of multi-media parallel multiply instructions is a multi-media parallel multiply and shift right instruction.

4. The method of claim 1 and further comprising:

applying a correction to factor to the integer result if at least one of the large integer operands are negative to produce a signed integer result.

5. The method of claim 4 wherein the signed integer result is in 2's complement format.

6. The method of claim 1 wherein at least one of the plurality of multi-media parallel multiply instructions forms at least two partial products of the series of partial products.

7. A method of performing 32-bit and 64-bit integer multiply operations in a processor adhering to the IA-64 architecture comprising:

manipulating 32-bit or 64-bit input operands to position 16-bit segments of the 32-bit or 64-bit input operands into register positions used as source fields by multi-media multiply instructions that perform 16-bit multiply operations in parallel;

executing a plurality of multi-media parallel multiply instructions to form a series of partial products, with at least one multi-media parallel multiply instruction forming at least two partial products of the series of partial products; and

adding the partial products together to produce a 32-bit or 64-bit integer result.

8. The method of claim 7 wherein at least one of the plurality of multi-media parallel multiply instructions is a multi-media parallel multiply and shift right instruction.

9. The method of claim 8 wherein the multi-media parallel multiply and shift right instruction is a pmpyshr2.u instruction.

10. The method of claim 7 and further comprising:

applying a correction to factor to a 64-bit integer result if either or both of the first of second 32-bit or 64-bit input operands are 32-bits and are negative, to produce a signed 64-bit integer result.

11. A computer program product, comprising:

at least one computer usable medium having computer readable code embodied therein for causing a CPU to perform integer multiply operations on large integer operands having a first number of bit positions using multi-media instructions that only support parallel multiply operations for small operands having a second number of bit positions, wherein the first number is at least twice as large as the second number, the computer program product including:

first computer readable program code devices configured to cause the CPU to manipulate the large integer operands to position segments of the large integer operands into register positions used as source fields by the multi-media instructions;

second computer readable program code devices configured to cause the CPU to execute a plurality of multi-media parallel multiply instructions to form a series of partial products; and

third computer readable program code devices configured to cause the CPU to add the partial products together to produce an integer result having at least the first number of bit positions.

12. The computer program product of claim 11 wherein the first number of bit positions is 32 or 64, and the second number of bit positions is 16.

13. The computer program product of claim 11 wherein at least one of the plurality of multi-media parallel multiply instructions is a multi-media parallel multiply and shift right instruction.

14. The computer program product of claim 11 and further comprising:

fourth computer readable program code devices configured to cause the CPU to apply a correction to factor to the integer result if at least one of the large integer operands are negative to produce a signed integer result.

15. The computer program product of claim 14 wherein the signed integer result is in 2's complement format.

16. The computer program product of claim 11 wherein at least one of the plurality of multi-media parallel multiply instructions forms at least two partial products of the series of partial products.

17. A computer program product, comprising:

at least one computer usable medium having computer readable code embodied therein for causing a CPU to perform 32-bit and 64-bit integer multiply operations in a processor adhering to the IA-64 architecture comprising, the computer program product including:

first computer readable program code devices configured to cause the CPU to manipulate 32-bit or 64-bit input operands to position 16-bit segments of the 32-bit or 64-bit input operands into register positions used as source fields by multi-media multiply instructions that perform 16-bit multiply operations in parallel;

second computer readable program code devices configured to cause the CPU to execute a plurality of multi-media parallel multiply instructions to form a series of partial products, with at least one multi-media parallel multiply instruction forming at least two partial products of the series of partial products; and

third computer readable program code devices configured to cause the CPU to add the partial products together to produce a 32-bit or 64-bit integer result.

18. The computer program product of claim 17 wherein at least one of the plurality of multi-media parallel multiply instructions is a multi-media parallel multiply and shift right instruction.

19. The computer program product of claim 18 wherein the multi-media parallel multiply and shift right instruction is a pmpyshr2.u instruction.

20. The computer program product of claim 17 and further comprising:

fourth computer readable program code devices configured to cause the CPU to apply a correction to factor to a 64-bit integer result if either or both of the first of second 32-bit or 64-bit input operands are 32-bits and are negative, to produce a signed 64-bit integer result.